What is clamed is:

1. A method of sampling an unknown clock signal using a known clock signal, comprising:

forming from the unknown clock signal a derived clock signal;

forming a sequence of multiple delayed versions of the derived clock signal, each delayed version following a first delayed version in the sequence being delayed more than a previous delayed version in the sequence;

for each delayed version of the derived clock signal:

sampling the delayed version of the derived clock signal at successive times defined by the known clock signal to produce first intermediate values; and

performing transition detection using the first intermediate values to produce second intermediate values; and

combining second intermediate values to produce sample values.

2. The method of claim 1, wherein combining comprises summing the second intermediate values.

3. The method of claim 2, wherein combining comprises mapping a sum of the second intermediate values to a smaller number of values.

4. The method of claim 4, wherein mapping is performed in accordance with an anticipated frequency range of the unknown clock signal.

5. A circuit for sampling an unknown clock signal using a known clock signal, comprising:

circuitry for deriving from the unknown clock signal to a derived clock signal;

a delay chain of logic elements, coupled to the derived clock signal and the unknown clock signal, for forming a sequence of multiple delayed versions of the derived clock signal, each delayed version following a first delayed version in the sequence being delayed more than a previous delayed version in the sequence;

multiple sampling chains of logic elements, each coupled to one of the multiple delayed versions of the derived clock signal and to the known clock signal;

multiple transition detection circuits, each coupled to one of the sampling chains such that, for each time a logic level of a delayed version of the derived clock signal is different at successive sampling times of the known clock signal, a transition detection circuit produces as an output signal thereof a transition indication value; and

a combining circuit for logically combining output signals of the transition detection circuits.

6. The apparatus of claim 5, wherein the combining circuit comprises a summation element for forming a sum of transition values and decision logic for comparing the sum to a threshold value.

7. The apparatus of claim 6, wherein the threshold value is set in accordance with an anticipated frequency range of the unknown clock signal.

8. A method of forming a number stream representing frequency or phase of digital or digitized clock signals using a digital circuit, one of the clock signals being a known clock signal and another of the clock signal being an unknown clock signal, comprising:

applying to the digital circuit an alias value indicating an expected frequency range of the unknown clock signal; and

forming the number stream in accordance with the alias value.

9. A digital circuit for forming a number stream for representing frequency or phase of digital or digitized clock signals, one of the clock signals being a known clock signal and another of the clock signal being an unknown clock signal, comprising:

a first logic section including multiple chains of flip flops, each chain producing an intermediate values; and

a second logic section for receiving an alias value indicating an expected frequency range of the unknown clock signal and combining the intermediate values to form the number stream.